

JC654 U.S. PTO  
09/752538  
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ISSUE CLASSIFICATION	
Class	Subclass

## U.S. UTILITY Patent Application

<i>Wkm</i> O.I.P.E. SCANNED <i>81</i> Q.A. <i>TC</i>	PATENT DATE
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APPLICATION NO. 09/752538	CONT/PRIOR	CLASS 174	SUBCLASS 262	ART UNIT 2847	EXAMINER CUNEO	I PATEL
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Stephen Ohr

Layered circuit boards and methods of production thereof

PTO-2040  
12/88

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
	<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.			<b>NOTICE OF ALLOWANCE MAILED</b>	
				<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____			<b>ISSUE FEE</b>	
	_____ (Assistant Examiner) _____ (Date)			Amount Due	Date Paid
	_____ (Primary Examiner) _____ (Date)			<b>ISSUE BATCH NUMBER</b>	
	_____ (Legal Instruments Examiner) _____ (Date)				

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